AMENDMENTS TO THE CLAIMS

This version of the claims replaces and supercedes all prior versions of the claims.

1. – 19. (Canceled)

20. **(Withdrawn)** A computer-readable recording medium on which is recorded a program for causing a computer to execute designing a system LSI circuit having a plurality of processor functions for executing a plurality of instruction sets, said program comprising:

(a) dividing system LSI circuit design specifications into hardware design and software design at a function designing stage;

(b) receiving, in hardware design, as hardware information, hardware configurations corresponding to respective ones of the plurality of processors, and the system instruction and the plurality of instruction sets described at an algorithm level; and

(c) performing behavioral synthesis using the hardware information, wherein said processor includes:

a system instruction decoder, provided separately of the plurality of processor functions, for decoding a system instruction that is not executed by any of the plurality of processor functions; and

a system instruction execution unit for selecting one of the plurality of processor functions in response to the system instruction decoded by said system instruction decoder.

21. – 22. (Canceled)

23. (Currently Amended) A processor that performs a first instruction set and a second instruction set, comprising:

a first execution controller executing a first decoded result being a decoded signal of an

instruction included in the first instruction set;

a second execution controller executing a second decoded result being a decoded signal of an instruction included in the second instruction set, the second execution controller being set up independently from the first execution controller;

a first arithmetic unit performing an arithmetical operation relative to execution of only the first decoded result; and

a shared arithmetic unit operatively coupled in common to the first and second execution controllers to perform arithmetical operations relative to execution of the first decoded result and the second decoded result,

wherein the first execution controller executes the first decoded result by using both the first arithmetic unit and the shared arithmetic unit.

24. (Previously Presented) The processor according to claim 23, further comprising:

a first decoder that generates the first decoded result by decoding the instruction included in the first instruction set; and

a second decoder that generates the second decoded result by decoding the instruction included in the second instruction set.

25. (Canceled)

26. (Previously Presented) The processor according to claim 23, further comprising:

a common instruction set decoder that decodes a common instruction included commonly in the first and second instruction sets.

27. (Currently Amended) The processor according to claim 24, further comprising:

a pipeline stage that is provided between the first decoder and ~~the~~ a first processing unit.

28. (Currently Amended) The processor according to claim 24, further comprising:

a first pipeline stage provided between the first decoder and ~~the~~ a first processing unit;

and

a second pipeline stage provided between the second decoder and ~~the~~ a second processing

unit.

29. (Currently Amended) The processor according to claim 28, wherein said first pipeline stage

has a different number ~~from~~ of stages than said second pipeline stage.

30. (Currently Amended) The processor according to claim 27, wherein ~~said stage~~ a number of

stages of the first pipeline stage is variable.

31. (Currently Amended) The processor according to claim 28, wherein ~~the stage~~ a number of

the first and second ~~pipelines~~ pipeline stages are variable.

32. (Currently Amended) The processor according to claim 24, further comprising a system

instruction decoder that decodes a system instruction ~~which~~ and selects use of ~~any~~ one of the first

and second decoders based on the system instruction.

33. (Previously Presented) The processor according to claim 32, wherein said system

instruction decoder is provided separate from the first and second decoders.

34. (Previously Presented) The processor according to claim 24, wherein any one of the first

and second decoders is selected for use in response to an interrupt signal.

35. (Previously Presented) The processor according to claim 32, wherein said system

instruction includes at least one of instructions for setting power voltage and/or operating rate at

which the processor operates.

36. (Previously Presented) The processor according to claim 23, further comprising:

a memory that stores both the first and second decoded results.

37. – 40. (Canceled)

41. (Previously Presented) The processor according to claim 23, further comprising:

a first register file operating with regard to execution of only the first decoded result; and

a shared register file operating with regard to execution of the first decoded result or the second decoded result.

42. (Previously Presented) The processor according to claim 41, further comprising:

a second arithmetic unit performing an arithmetical operation relative to execution of only the second decoded result; and

a second register file operating with regard to execution of only the second decoded result.

43. – 46. (Canceled)

47. (Currently Amended) A processor comprising:

a first decoder decoding a first instruction to output a first decoded result without decoding a second instruction;

a second decoder decoding the second instruction to output a second decoded result without decoding the first instruction;

a first execution controller coupled to the first decoder to transmit a first control signal in response to the first decoded result from the first decoder;

a second execution controller coupled to the second decoder to transmit a second control signal in response to the second decoded result from the second decoder;

a first arithmetic unit coupled to the first execution controller to operate with regard to execution of the first decoded result in response to the first control signal, said first arithmetic unit being not responsive to the second control signal from the second execution controller;

a shared arithmetic unit operatively coupled to the first and second execution controllers

to operate with regard to execution of the first and second decoded results in response to one of the first and second control signals,

wherein the first execution controller executes the first decoded result by using both the first arithmetic unit and the shared arithmetic unit.

48. (Previously Presented) The processor according to claim 47, further comprising:

a second arithmetic unit coupled to the second execution controller to operate with regard to an execution of the second decoded result in response to the second control signal without responding to the first control signal from the first execution controller.

49. (Previously Presented) The processor according to claim 47, wherein

the first arithmetic unit and the shared arithmetic unit receive the first control signal from the first execution controller at the same time.

50. (Canceled)